



H.100 Hardware Compatibility Specification : CT Bus

revision 1.0

Abstract. This document represents an interoperability agreement among hardware developers. It seeks to simplify the challenges for system developers and integrators that wish to use mixed hardware platforms or to provide portability across hardware platforms.



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About ECTF

As Computer Telephony (CT) becomes an integral part of the entire communications network including the Internet, there are increasing challenges to making diverse communication products work together. The ECTF is focused on solving the technical challenges of interoperability for the benefit of users and developers alike.

Founded in 1995, the ECTF is a non-profit organization composed of Computer Telephony suppliers, developers, systems integrators, and users from the Americas, Europe, and Asia/Pacific. Together we discuss, develop, and test approaches to successful multilayer interoperation within the PSTN, IP, and enterprise information system environments. Successful multilayer interoperation enables application solutions that can exploit the full range of contemporary communications capabilities while lowering costs for both developers and users.

The ECTF Technical Committee has worldwide scope and addresses global technical needs for:

- Convergence of computing and telephony
- Interoperability of defacto and de jure computer telephony standards
- Consistency of computer telephony interfaces
- Availability of scalable, networked, extensible computer telephony platforms and applications

Its goals are as follows:

- Provide architectural frameworks for interoperability
- Foster efficient and effective development of computer telephony products and services
- Facilitate industry acceptance of interoperability through non-ambiguous common implementation agreements
- Promote industry cooperation and exchange

The Technical Committee has a number of working groups (WGs) and task groups that underscore the areas of ECTF interest, such as:

- Administrative Services
- Application Interoperability
- Architecture
- Call Control Interoperability
- Computer Telephony Services Platform
- Hardware Components Interoperability

If you are a developer or a user of Computer Telephony products and services, we invite you to join the ECTF and help influence the direction and growth of the Computer Telephony Industry.

Reference Information

The cited references contain provisions which, through reference in this specification, constitute provisions of this specification. At the time of publication, the indicated versions in the following references were valid.

- *ECTF Architectural White Paper*, Enterprise Computer Telephony Forum.
- *ANSI/VITA 6-1994 Signal Computing Architecture*, VITA.
- *MVIP-90*, GO-MVIP.
- *PCI Specification*, revision 2.1, PCI Special Interest Group.
- *GR-1244-CORE*, section 3, issue 1, Bellcore, June 1995.
- *H-MVIP*, release 1.1, GO-MVIP.
- *Accunet T1.5(R) Service, Description and Interface Specification*, [TR 62411], AT&T, December 1990.

Contents

About ECTFiii
Reference Informationiv
Contentsv
Section 1 : CT Bus Overview	1
1.1 Objectives	1
1.2 Introduction	1
1.2.1 System Structural Model	1
1.3 Specification Terminology	2
1.4 Specification Diagrams	3
1.5 Signal Definitions	3
1.5.1 Core Signals	3
1.5.2 Compatibility Signals	4
1.5.3 Optional Signals	4
1.5.4 Reserved Signals	5
Section 2 : CT Bus Clocks and Synchronization	7
2.1 Introduction	7
2.2 CT Clock Signals	7
2.3 CT Clock Accuracy	8
2.4 CT_NETREF	8
2.5 Clock Fallback	9
2.5.1 Requirements for Masters and Slaves	9
2.5.2 Clock Fallback Behavior	10
Section 3 : Data Transfer Bus	13
3.1 Introduction	13
3.2 Data Bus Lines	13
3.3 Interface Device Requirements	14
3.4 Data Bus Timing	14
3.5 Other Timing Requirements	16

3.5.1	Clock Skew Requirements	16
3.5.2	Reset and Power On Timing	17
Section 4	: Electrical Specifications	19
4.1	Introduction	19
4.2	Interface Requirements	19
4.3	Terminations	20
Section 5	: Mechanical Specifications	23
5.1	Introduction	23
5.2	Connectors	23
5.3	Location	23
5.4	Pin Assignment	26
5.5	PCB Layout and Considerations	27
5.6	Cable	27
5.7	Transition PCBs	28
Section 6	: Partial Implementations	29
6.1	Introduction	29
6.2	Requirements for Partial Implementations	29
Section 7	: Optional Signals	31
7.1	Introduction	31
7.2	Message Channel	31
7.2.1	Introduction	31
7.2.2	Message Bus Lines	31
7.2.3	Message Bus - Timing Rules and Observations	32
7.2.4	Bus Drivers and Receivers	33
7.2.5	Bus Terminations	33
7.2.6	DC Characteristics	34
7.2.7	Loading Limitations	35
7.3	CT_+5Vdc	35

Section 8 : Inter-operation with Other Busses	37
8.1 Introduction	37
8.2 Common Requirements	37
8.3 H-MVIP	39
8.3.1 Clocks	40
8.4 SCbus	41
8.4.1 Signal Cross Reference	41
8.4.2 Clock Compatibility	41
Appendix A : V/I Curves for 24mA Drivers Used in CT Bus Simulations	43



Section 1 : CT Bus Overview

1.1 Objectives

The integration of computers and telecommunications has enabled a wide range of new communications applications and has fueled an enormous growth in communications markets. A key element in the development of computer-based communications equipment has been the addition of an auxiliary telecom bus to existing computer systems. Most manufacturers of high-capacity computer-based telecommunications equipment have incorporated some such telecom bus in their systems. Typically these buses transport and switch Nx64 Kbps low-latency communications traffic between boards within the computer, independent of the computer's I/O and memory buses. At least a half dozen of these PC-based telecom buses are in volume use within equipment based on ISA/EISA and MCA computers.

The objective of this CT Bus specification is to provide a single telecom bus for the entire industry. This specification is intended to provide all the necessary information to implement a CT Bus interface at the physical level. Adoption of a single bus will facilitate the inter-operation of components, thus providing maximum flexibility to equipment manufacturers, value-added resellers, system integrators and others building computer-based telecommunications applications. A single, industry-wide, CT Bus will drive new applications, reduce costs and expand markets.

To facilitate its adoption, the CT Bus is initially targeted at PCI form-factor add-in boards. The CT Bus specification is being released fairly early in the life cycle of PCI products and before many of the ISA/EISA/MCA telecom buses have been carried over to PCI form-factor products. The CT Bus might be extended to other computer form-factors in the future.

To further aid its widespread adoption, CT Bus has been designed to support easy inter-operation with the following telecom buses: the MVIP-90 and H-MVIP buses from GO-MVIP (Global Organization for MVIP, Washington DC) and the SCbus from Dialogic Corporation (Parsippany, New Jersey).

Finally, CT Bus has been designed with more capacity than any of the previously deployed buses, so as to support the next generation of high capacity servers. At the same time, CT Bus includes well-defined subsets so that economical low-end systems can be built involving as few as two boards.

1.2 Introduction

1.2.1 System Structural Model

Figure 1-1 shows all of the components and interfaces in the ECTF architecture. Interfaces are depicted by trapezoids with the defined side of the interface being the longest side of the trapezoid.

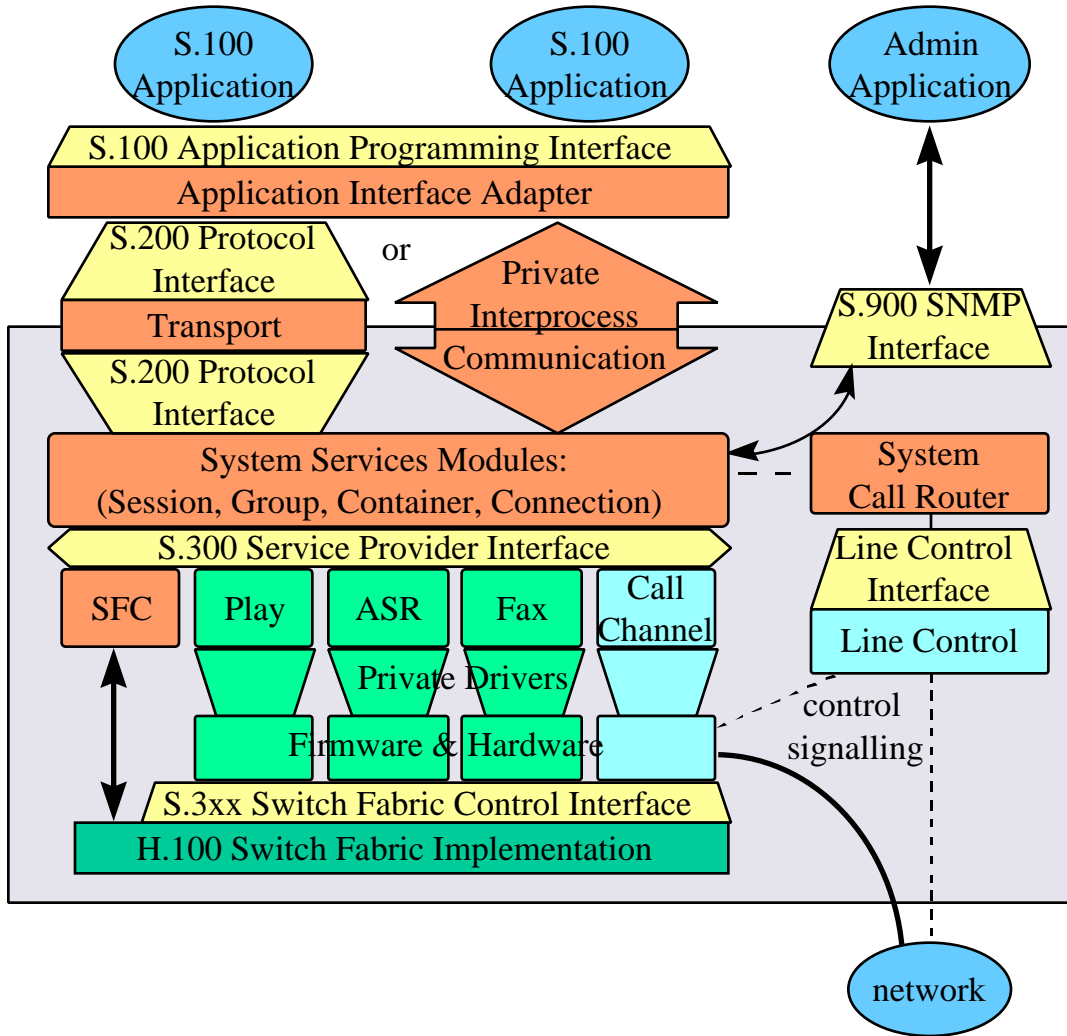


Figure 1-1 ECTF Architectural Model - Basic CT Media Server Configuration

This specification defines the actual ribbon cable and time-slots section of the ECTF Architectural Model. This is a physical layer specification only. (See Ref. 1).

1.3 Specification Terminology

The specification contains requirements, options, suggestions and informative text.

Requirements are identified by the reserved upper case words "MUST" or "MUST NOT" in the text. Requirements MUST be implemented to be considered compliant with the specification. In tabular data, "Min" and "Max" are equivalent to "MUST".

Options are identified by the reserved upper case words “MAY” in the text. Implementation of these options is up to the developer. However, if they are implemented they **MUST** be implemented according to the specification.

Recommendations are identified by the reserved upper case words “SHOULD” or “SHOULD NOT” in the text. Recommendations describe the preferred approach on a given topic. The developer will understand the implications of not following a given recommendation before adopting an alternative approach. In tabular data “Typ” is equivalent to “SHOULD”.

1.4 Specification Diagrams

As aids to defining or describing CT Bus, system or software operation several types of diagrams are used, including:

- Timing diagrams: Show the timing relationships between signal transitions. The times specified will have minimum and/or maximum limits associated with them. Some of the times included on these diagrams specify the behavior of the bus interface logic while other times specify the interlocked behavior of the associated functional interfaces.
- Sequence diagrams: Show only the interlocked timing relationships of the functional interfaces. This diagram is intended to show a sequence of events rather than to specify the times involved.

1.5 Signal Definitions

There are four classes of signals on the CT Bus, **Core** signals, **Compatibility** signals, **Optional** signals, and **Reserved** signals. **Core**, **Compatibility**, and **Reserved** signals are required.

1.5.1 Core Signals

Core signals are required CT Bus signals. These signals **MUST** be implemented exactly as described.

/CT_FRAME_A Frame Sync - driven by the “A” clock master. This is a negative true pulse, nominally 122 nS wide that straddles the beginning of the first bit of the first time-slot. /CT_FRAME_A has a period of 125uS.

CT_C8_A Bit Clock - driven by “A” clock master. The clock frequency is 8.192MHz. The duty cycle of this signal is nominally 50%.

/CT_FRAME_B Redundant Frame Sync - driven by the “B” clock master. This is a negative true pulse, nominally 122 nS wide that straddles the beginning of the first bit of the first time-slot. /CT_FRAME_B has a period of 125uS.

CT_C8_B Redundant Bit Clock - driven by “B” clock master. The clock frequency is 8.192 MHz. The duty cycle of this signal is nominally 50%.

CT_D[0:31] Serial Data lines that can be driven by any board in the system. However, only one board can drive the bus at any given time-slot on each stream. Each signal contains 128 time-

slots per frame at a clock frequency of 8.192MHz. These 32 signals collectively are referred to as the CT_D bus. CT Bus devices MAY connect to subsets of the CT_D bus. (See Section 6).

CT_NETREF Secondary Network Timing Reference - driven by any (single) CT Bus digital trunk interface to provide backup network synchronization to the CT Bus. This signal can have any duty cycle as long as the period is 125 uS (8kHz), 647nS (1.544MHz), or 488nS (2.048MHz) and is network synchronized. There is no specified phase relation between CT_NETREF and the other clock signals. CT_NETREF has a minimum high of 90 nS and a minimum low time of 90 nS.

1.5.2 Compatibility Signals

Compatibility signals MUST be implemented by all bus master-capable cards but are present only to guarantee inter-operation with SCbus, MVIP-90, or H-MVIP. The behavior of these signals will track their usage in those specifications.

/FR_COMP Compatibility frame pulse - driven by current clock master. This is a negative true pulse, nominally 122 nS wide, that straddles the beginning of the first bit of the first time-slot. /FR_COMP has a period of 125uS. This signal serves as the frame synchronization signal for SCbus (Fsync*) and MVIP (/F0).

SCLK SCbus System clock - driven by current clock master. The clock is selectable. It can be either 2.048M, 4.096M, or 8.192MHz. SCLK is used to identify the data bit positions on the SCbus. The positive going edge indicates the beginning of the bit. (See Ref. 2).

SCLKx2* SCbus System (**SCLK**) clock times two - driven by current clock master. The clock frequency is exactly twice that of SCLK. Transitions of SCLK occur on the falling edge of SCLKx2* for SCbus operating at 2.048MHz or 4.096MHz. (See Ref. 2). See section 8.4.2 for SCLKx2* timing for SCbus operating at 8.192MHz.

C2 MVIP-90 bit clock - driven by current clock master. The clock frequency is 2.048 MHz, nominally symmetrical. The positive going edge indicates the beginning of the bit. (See Ref. 3).

/C4 MVIP-90 bit clock times two - driven current by clock master. The clock frequency is exactly twice C2, and transitions of C2 are synchronous with the falling edge of /C4. (See Ref. 3).

/C16+, /C16- H-MVIP 16 MHz Clock - driven by current clock master. This differential signal is used to read and write bits on the serial data lines by H-MVIP cards. (See Ref. 6).

1.5.3 Optional Signals

Optional signals MAY be implemented on the CT Bus. However, if they are implemented, they MUST conform to this specification. Interfaces that do not implement these signals MUST NOT connect to them and MUST NOT use the lines for other purposes.

CT_MC Message Channel. This open collector, bit-serial bus is shared by all equipped CT bus interfaces for inter-device communications. This signal is terminated on each CT Bus interface in the system which has message bus capability.

CT_+5Vdc This signal, if present, is used to provide power to active transition devices.

1.5.4 Reserved Signals

These signals are reserved for future use. CT Bus interfaces **MUST NOT** connect to these signals



Section 2 : CT Bus Clocks and Synchronization

2.1 Introduction

Figure 2-1 shows the functional timing relationship of the CT Bus clocks and /CT_FRAME signals. The /CT_FRAME signals are nominally 122ns long centered around the beginning of the first bit cell. For compatibility, CT Bus clock masters MUST be able to generate /CT_FRAME(A/B), CT_C8(A/B), /FR_COMP, C2, /C4, /C16(, SCLK, and SCLKx2*. See Section 8 for details. /CT_FRAME signals A and B and CT_C8 signals A and B have nominally identical timing and will be referred to as /CT_FRAME and CT_8. Where the “A” and “B” signals have different behavior, they will be explicitly referred to with the “A” and “B” designations. CT Bus slaves SHOULD derive all timing from /CT_FRAME and CT_C8 only.

Master clock capability MUST be provided on any board that contains an interface to an external communications network.

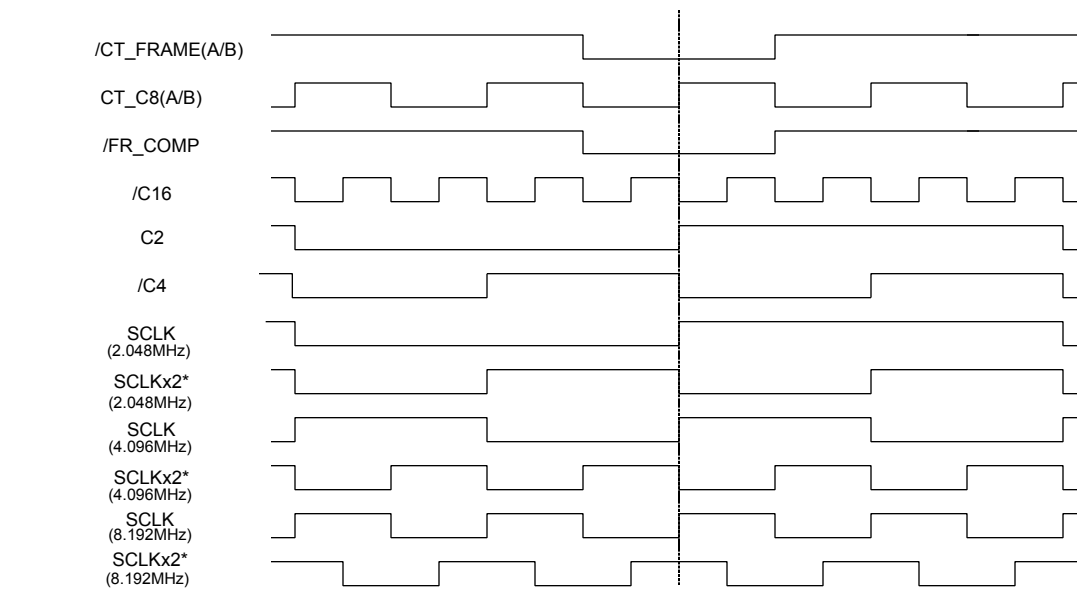


Figure 2-1 Clock Alignment

2.2 CT Clock Signals

Figure 2-2 shows the required clock signals on the CT Bus. The /CT_FRAME signal is nominally centered around the rising edge of CT_C8. All timing measurements are based on this rising edge.

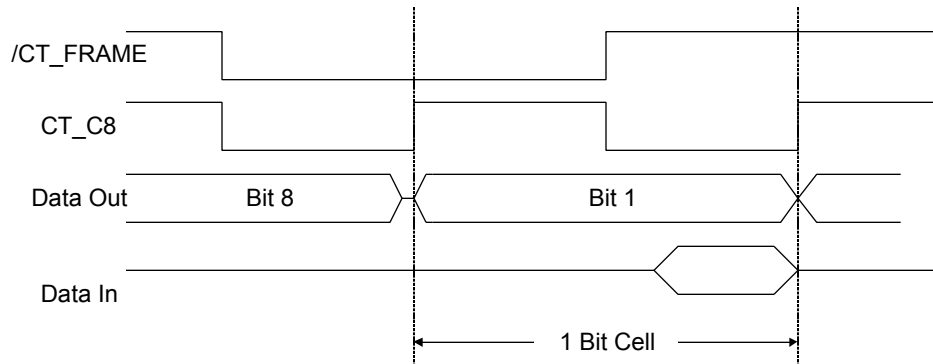


Figure 2-2 Detailed Functional Timing

2.3 CT Clock Accuracy

All clocks generated by CT Bus clock masters **MUST** meet Stratum 4 Enhanced (or international equivalent) for network connected applications and Stratum 4 (or international equivalent) for termination or stand-alone applications. (See Ref. 5 and Ref. 7).

2.4 CT_NETREF

CT_NETREF provides an additional network timing reference. The master clock for the CT Bus is synchronized to the primary reference digital trunk. The signal CT_NETREF **MUST** be synchronized to the secondary reference digital trunk. In the event that the primary trunk fails, the phase locked loop (PLL) on Card 1 (CT Bus clock master) will switch to CT_NETREF to derive its frequency. Under these conditions, clocks on the CT Bus **MUST NOT** violate timing requirements of section 2.3, and slave cards **MUST** continue to run unaffected by the failure of the primary reference. CT Bus digital trunk interfaces **MUST** be able to extract PSTN timing and drive CT_NETREF at 8kHz. In addition to the capability to drive CT_NETREF at 8kHz, a board **SHOULD** have the capability to drive CT_NETREF at 1.544MHz and/or 2.048MHz. When more than one CT_NETREF rate is supported, the choice **MUST** be under software control. CT Bus master-capable boards **MUST** be able to utilize the CT_NETREF signal at 8kHz. In addition to the capability to utilize 8kHz, all master-capable boards **SHOULD** have the capability to utilize 1.544MHz and/or 2.048MHz.

The ability to drive the CT_NETREF signal **MUST** be provided on any board that is capable of deriving reference timing from an external network. Typically, this will be an external digital telecommunications network. CT_NETREF **MUST** have a slew rate of less than 0.3 V/ns. In cases where the CT Bus is synchronized to the PSTN, CT_NETREF is frequency locked to CT Bus clocks by virtue of its source in the PSTN. CT_NETREF has no specific phase with respect to other CT Bus clocks. The active edges of CT_NETREF can occur anywhere within a frame.

CT_NETREF MUST be network synchronized. CT_NETREF MUST NOT be driven if its network reference has failed. Failure criteria for loss of network reference is determined by the applicable standards for the network interface type. Figure 2-3 shows how this signal is used.

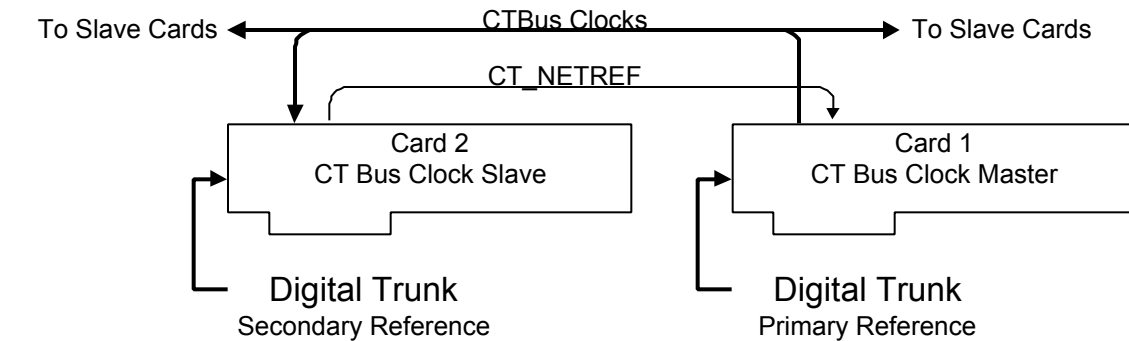


Figure 2-3 CT_NETREF Operation

2.5 Clock Fallback

CT Bus provides dual clock/frame signals for current master hot-swap and clock driver failure situations. This section contains the requirements for CT Bus clock masters and slaves.

2.5.1 Requirements for Masters and Slaves

CT Bus clock masters MUST implement all of the clock fallback features described in this section. CT Bus slaves MAY participate in the clock fallback mechanism. If they do so, they MUST implement all of the clock fallback features described in this section.

Requirements in this section mandate that all CT Bus interfaces (masters and participating slaves) be able to assess the quality of CT Bus core clocks (CT_C8 and /CT_FRAME). All CT Bus interfaces MUST use the following criteria to assess the quality of CT Bus core clocks. At a minimum, these clocks MUST be considered as unreliable if either of the following two conditions are detected:

1. A received rising edge of CT_C8 does not arrive within (35ns of the expected time of that edge; or
2. There are not exactly 1024 clock periods per frame.

The following capabilities MUST be provided by CT Bus masters and participating slaves:

1. They MUST monitor both the “A” and “B” clocks according to the criteria described above.
2. They MUST be able to report, under program control, the presence of unreliable clocks to the host.
3. If a master-capable or participating slave card detects that the current master clock or frame is unreliable, they MUST be able to do both of the following:

- a. Switch automatically to the designated secondary clock and frame, if enabled to do so by software; and
- b. Switch to the designated secondary clock and frame by software command.

2.5.2 Clock Fallback Behavior

Figure 2-4 shows the system clocking model. Initially, the designated primary clock master drives the “A” clock and frame signals, and the designated secondary master drives the “B” clock and frame signals. After fallback their roles are reversed, i.e. the “B” clocks will be serving as primary master clocks, and a new “A” clock source will be serving as the designated secondary clock source. CT_NETREF is shown as coming from a third digital trunk, but it can be sourced by any card that can provide a network derived reference, e.g. a Building Integrated Timing Supply (“BITS” - See Ref. 5).

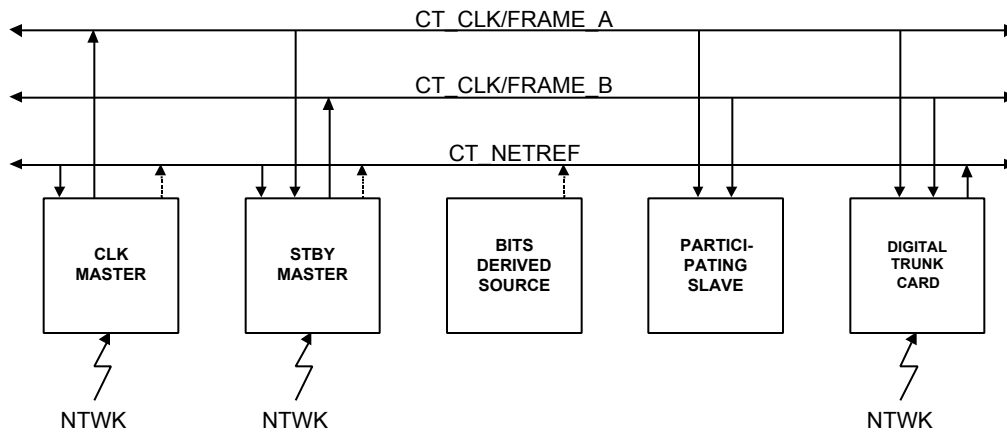


Figure 2-4 System Clocking Model

Figure 2-5 shows the states and transition conditions of the clock fallback procedure.

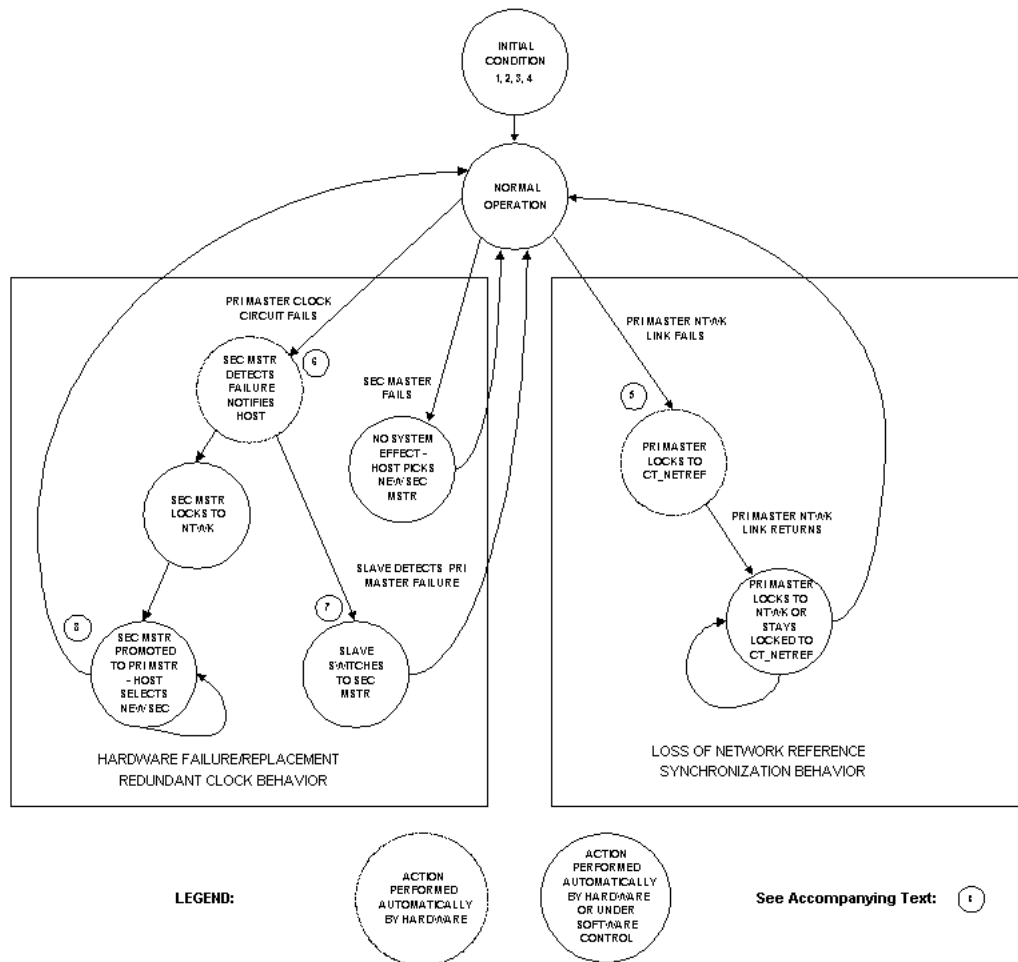


Figure 2-5 Clock Fallback State Diagram

The procedure below **MUST** be implemented as described.

1. One card is initially designated “primary” master and drives “A” clocks.
2. Another card is initially designated “secondary” master and drives the “B” clocks. The “B” clocks **MUST** be edge-synchronous with the “A” clocks.
3. All other cards, by virtue of software instruction, initially listen to “A” clocks.
4. A card with a network-derived reference is selected to drive CT_NETREF. In order to provide the secondary network timing reference CT_NETREF **MUST** be derived from a digital trunk other than the trunk providing the reference for the “A” master. (See Sect. 2.4).
5. The “A” master has the responsibility to monitor its on-board network derived reference. If the network derived reference becomes unreliable, the “A” master **MUST** continue sourcing “A” clocks in stable holdover mode until it automatically makes a Stratum 4 Enhanced compatible switch to CT_NETREF for its network timing reference. When the

on-board network timing reference comes back, the “A” master makes an Stratum 4 Enhanced compatible switch back to the on-board network derived reference, if enabled to do so by software. This covers the “primary master has lost network timing” case and the associated Stratum 4 Enhanced requirements.

6. All master capable and participating slave interfaces **MUST** have the capability to monitor “A” and “B” clocks. If the “A” clock becomes unreliable, system software **MUST** be notified by a master-capable or participating slave board. More than one master-capable or participating slave board **MAY** provide the notification to system software. Either autonomously, or by virtue of system software instruction, the “B” master switches (it **MAY** switch asynchronously) to a network-derived reference (or local oscillator if no network-derived reference is available), and continues to drive the “B” clocks.
7. All slave cards, automatically or by virtue of software instruction, switch (they **MAY** switch asynchronously) to “B” clocks. This covers the case where the “A” master has been removed for hot-swap, and the case where there is contention on the “A” clock or frame lines, which represent hardware failure modes and have no associated Stratum 4 Enhanced requirements. Any switch from “A” to “B” clocks (or vice versa) that is not due to an internal hardware failure **MUST** meet Stratum 4 Enhanced requirements.
8. System software designates a new “A” master and the system returns to the normal operation state, if enabled to do so by software, except now the roles of “A” and “B” are reversed. Now the “B” master is “primary” and “A” master is “secondary”.

Section 3 : Data Transfer Bus

3.1 Introduction

The CT Bus is a synchronous, bit-serial, TDM transport bus operating at 8.192MHz. It consists of two clocks, two frame sync pulses, one backup network timing reference, and 32 independent bit-serial data streams (CT_D[0:31]). Six additional clocks are sourced by CT Bus timing masters to insure compatibility with other TDM busses. Compatibility modes permit operation at 2.048, 4.096, and 8.192MHz as well. (See Section 8 for further discussion of inter-operation with other busses.)

The clock CT_C8 is used to define the bit positions. The frame sync pulse /CT_FRAME is used to indicate the frame boundary and occurs every 125 uS (8kHz). The CT_D bits between two consecutive frame pulses are divided, starting at the frame boundary, into multiple eight bit groups called time-slots. There are 128 time-slots in each frame. The total bandwidth of the bus is 32 streams x 8.192MHz clock rate = 262 Mbps.

3.2 Data Bus Lines

Each CT_D serial stream is divided into a 1024 bit group called a frame. Each frame is exactly 125 microseconds long. Each frame is then further divided, starting at the frame boundary, into a fixed number of eight bit sub-frames called time-slots. Each frame consists of 128 time-slots. The first eight bit group following the frame sync is designated as CT_Dx; TS0 (Data Stream x; Time-slot 0); the second eight bit group is CT_Dx; TS1 (Data Stream x; Time-slot 1) and so on. The MSB (sign bit) MUST be at the beginning (bit 1) of the time-slot for PCM data. For other data types (e.g. HDLC) the MSB MAY be first or last depending on the format. See figure 3-1.

Figure 3-1 Frame Structure

3.3 Interface Device Requirements

Any switching device(s) used on a CT Bus master-capable card needs to provide a minimal set of capabilities. The amount of switching between local card time-slots and CT Bus time-slots is determined by the requirements of the interface card itself. For example: a dual T1 card only needs to switch the 48 channels from the 2 T1 lines to any of the 4096 time-slots of the CT bus. Cards capable of being CT Bus clock masters **MUST** provide 128 time slots of switching from CT Bus data streams operating at 2, 4, or 8 Mbps to CT Bus data streams operating at 2, 4, or 8 Mbps, as a minimum. More switching **MAY** be provided at the vendors discretion.

The switching device(s) on the master-capable card **MUST** also provide 2 modes of operation, constant delay mode, and minimum delay mode. Minimum delay is used for 64kbps channels, and constant delay mode is used for Nx64kbps channels. Each 64kbps time-slot **MUST** be software programmable for these 2 modes of operation. This requirement applies to all switching combinations, i.e. local time-slots to CT Bus time-slots and CT Bus time-slots to CT Bus time-slots.

Slave cards **MAY** also be required to provide both constant and minimum switching modes. The requirement to provide this feature is determined by the function of the card. For example, POTS line cards would not provide constant and minimum delay, but a DSP card doing video conferencing would be required to have constant and minimum delay mode.

3.4 Data Bus Timing

Figure 3-2 shows the detailed timing of the clocks and data streams. There are a total of 32 data streams each operating at 8 MHz. Data is nominally sampled at the 3/4 point of the bit cell. In order to guarantee non-overlapped operation on the data bus, the last bit of time-slot N **MUST** be inactive before the first bit of time-slot N+1. Designs meeting the specified timing are guaranteed to be non-overlapping. Designs **MAY** implement sub-rate channels. The details of sub-rate implementations are beyond the scope of this document. However, boards implementing sub-rate channels **MUST** observe the timing requirements for time-slot boundaries regardless of the number of bits in the time-slot. That is, optional sub-rate switching **MUST** also guarantee non-overlapped operation at time-slot boundaries.

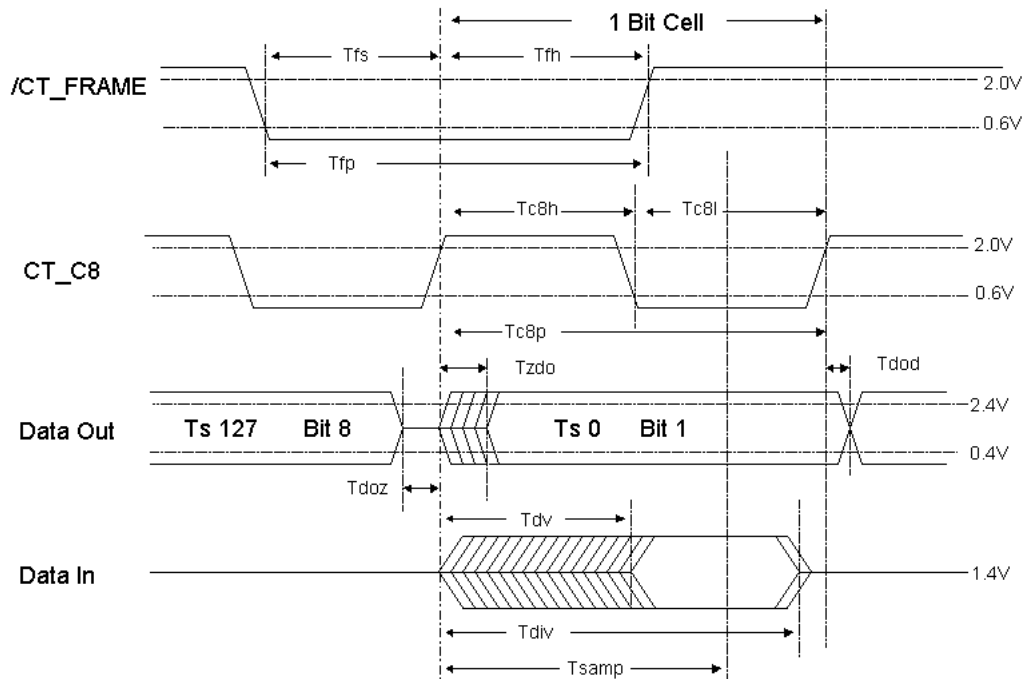

Figure 3-2 Detailed Data Bus Timing

Table 3-1 Component Timing Specification

Symbol	Parameter	Min	Typ	Max	Unit	Notes
	Clock edge rate (All Clocks)	0.25		2	V/ns	1
Tc8p	Clock CT_C8 Period	$122.066 - \Phi$		$122.074 + \Phi$	ns	5
Tc8h	Clock CT_C8 High Time	$49 - \Phi$		$73 + \Phi$	ns	6
Tc8l	Clock CT_C8 Low Time	$49 - \Phi$		$73 + \Phi$	ns	6
Tsamp	Data Sample Point		90		ns	9
Tdoz	Data Output to HiZ Time	-20		0	ns	3, 7, 11
Tzdo	Data HiZ to Output Time	0		22	ns	3, 7, 11
Tdod	Data Output Delay Time	0		22	ns	3, 7
Tdv	Data Valid Time	0		69	ns	3, 8, 10
Tdiv	Data Invalid Time	102		112	ns	
Tfp	/CT_FRAME Width	90	122	180	ns	
Tfs	/CT_FRAME Setup Time	45		90	ns	
Tfh	/CT_FRAME Hold Time	45		90	ns	

Table 3-1 Component Timing Specification (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Φ	Phase Correction	0		10	ns	12

Table Notes

1. The rise and fall times are determined by the edge rate in V/nS. A “Max” edge rate is the fastest rate at which a clock transitions. CT_NETREF has a separate requirement. (See section 2.4).
2. Measuring conditions, data lines
 - Vth (threshold voltage)=1.4V
 - Vhi (test high voltage)=2.4V
 - Vlo (test low voltage)=0.4V
 - Input signal edge rate=1 V/nS
 Measuring conditions, clock and frame lines
 - Vt+ (test high voltage)=2.0V
 - Vt- (test low voltage)=0.6V
 - Input signal edge rate=1 V/nS
3. Test Load - 200 pF
4. When RESET is active, every output driver is tristated.
5. Tc8p Min and Max are under free-run conditions assuming ± 32 ppm clock accuracy.
6. Non-cumulative, Tc8p requirements still need to be met.
7. Measured at the transmitter.
8. Measured at the receiver.
9. For reference only.
10. Tdv = Max. clock cable delay + Max. data cable delay + Max. data HiZ to output time = 12nS + 35nS + 22 nS = 69nS. Max. clock cable delay and max. data cable delay are worst case numbers based on electrical simulation.
11. Tdoz and Tzdo apply at every time-slot boundary.
12. Φ (Phase Correction) results from PLL timing corrections.

3.5 Other Timing Requirements

3.5.1 Clock Skew Requirements

Figure 3-3 and table 3-2 show the skew requirements between CT Bus “A” and “B” clocks and between CT Bus “A” clocks and the compatibility clocks.

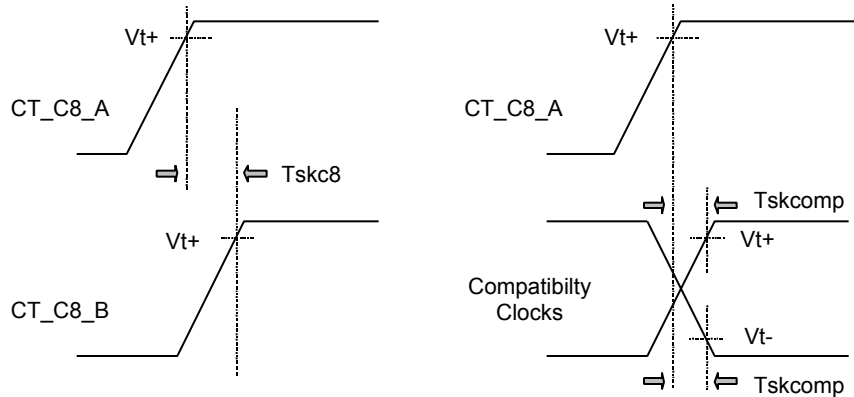

Figure 3-3 Clock Skew Timing

Table 3-2 Clock Skew Timing

Symbol	Parameter	Min	Typ	Max	Units	Notes
Tskc8	Max Skew between CT_C8 "A" and "B"			$\pm 10 \pm \Phi$	ns	1,2,3,4
Tskcomp	Max Skew between CT_C8_A and any compatibility clock			± 5	ns	1

Table Notes

1. Test Load - 200 pF.
2. Assumes "A" and "B" masters in adjacent slots.
3. When static skew is 10nS and, in the same clock cycle, each clock performs a 10nS phase correction in opposite directions, a maximum skew of 30nS will occur during that clock cycle.
4. Meeting the skew requirements in table 3-2 and the requirements of section 2.3 could require the PLLs generating CT_C8 to have different time constants when acting as primary and secondary clock masters.

3.5.2 Reset and Power On Timing

Devices which can drive CT Bus signals MUST asynchronously place all bus signals in tristate during reset or idle. Any CT Bus data signal MUST be able to be tristated under software control on a time-slot by time-slot basis. Table 3-3 shows the timing for Reset and Power On.

Table 3-3 Reset and Power On Timing

Symbols	Parameter	Min.	Typ	Max	Unit
Trd	Output float delay from reset active			1	us

Table 3-3 Reset and Power On Timing (continued)

Symbols	Parameter	Min.	Typ	Max	Unit
Trs	Reset active from power good		5		us

Section 4 : Electrical Specifications

4.1 Introduction

CT Bus is a bit-serial, byte oriented, synchronous, TDM bus. Voice/data transfer on the bus is accomplished by assigning one or more time-slot numbers and bus stream numbers (CT_Dn plus time-slot number) to the sender and receiver(s). At the selected time-slot, the software selected sender drives the bus and somewhere on the bus, the receiver(s) clocks in the data bits. There is no handshake or confirmation between the sender and the receiver(s). The operation is solely based on the assumption that all boards on the bus are under software control, use the bit clocks for bit registration, and perform frame alignment using the frame sync pulse (/CT_FRAME). By using devices with the drive characteristics listed below the DC characteristic requirements of the CT Bus can be met.

4.2 Interface Requirements

The drive specification assumes that a maximum of 20 loads (a load is considered to consist of one connector, one stub, and one I/O cell) can be connected to one line. More than 20 loads **MUST NOT** be connected to any line. More than 20 physical boards **MUST NOT** be attached to the CT Bus. In order to assure that the interleaved grounds on the ribbon cable act as effective grounds, there **MUST NOT** be more than 7 inches between populated CT Bus cards.

PCI-compliant data line I/O cells **MUST** be used for the CT Bus data lines. (See Ref.4, Chap. 4).

Tables 4 and 5 list the electrical requirements for CT_C8 and /CT_FRAME. See Appendix A for V/I curves used in CT Bus simulations of CT_C8 and /CT_FRAME.

Table 4-1 Electrical Drive Specifications - CT_C8 and /CT_FRAME Drivers

Symbol	Parameter	Condition	Min	Max	Unit	Note
Voh	Output high voltage	Iout = -24mA	2.4	5.25	V	
Vol	Output low voltage	Iout = -24mA	-0.25	0.4	V	

CT_C8 and /CT_FRAME receivers **MUST** have Schmitt-trigger inputs to reduce the sensitivity to discontinuities on these lines.

Table 4-2 Electrical Specifications - CT_C8 and /CT_FRAME Receivers

Symbol	Parameter	Condition	Min	Max	Unit	Note
Vt+	Positive-going Threshold		1.2	2.0	V	
Vt-	Negative-going Threshold		0.6	1.6	V	
Vhys	Hysteresis (Vt+ - Vt-)		0.4		V	

Table 4-2 Electrical Specifications - CT_C8 and /CT_FRAME Receivers (continued)

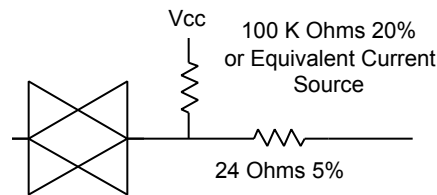
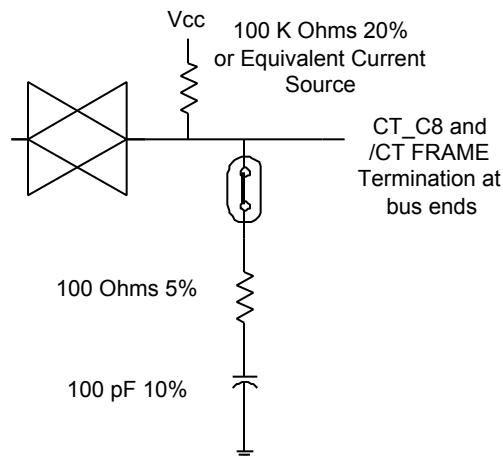
Symbol	Parameter	Condition	Min	Max	Unit	Note
Cin	Input pin capacitance			10	pF	

4.3 Terminations

Each CT Bus device **MUST** provide a 100 K Ω pull-up to +5Vdc (or current source equivalent) on all CT Bus lines.

Each CT Bus device **MUST** provide a 24 Ω series termination on all CT Bus lines except CT_C8 and /CT_FRAME. This series termination **SHOULD** be placed as close as possible to the connector. The 100K pull-up resistor or current source **MUST** appear on the I/O cell side of the series termination.

The signals CT_C8 and /CT_FRAME **MUST** have a configurable termination consisting of a 100 Ω /100 pF AC termination network at the physical ends of the bus. See figures 4-1,4-2, and 4-3 for termination schematics. It **MUST** be possible to enable or disable this termination at installation time. In a configured system, only the boards at the ends of the bus **MUST** have their configured terminations enabled. All other boards **MUST NOT** have their terminations enabled.


Figure 4-1 Data Line Termination

Figure 4-2 Clock Line Termination at Ends of Bus

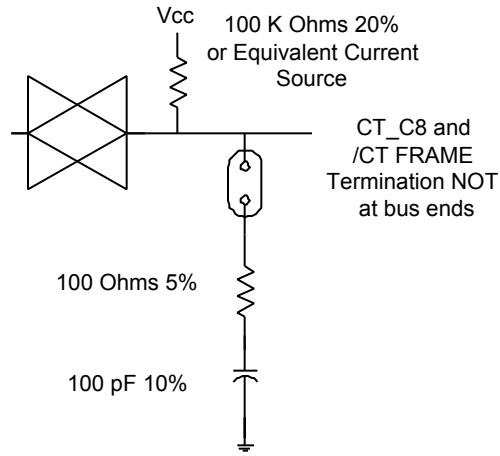


Figure 4-3 Clock Line Terminations at Points Other than Ends of Bus



Section 5 : Mechanical Specifications

5.1 Introduction

The CT Bus is defined on PCI form factor printed circuit boards (PCB). The dimensions of this format can be found in the PCI Specification Rev. 2.1.(See Ref. 4). Note that the PCI specification does not make any recommendations nor place any limitations on the location of mezzanine connectors along the top of the PCB. As long as the entire connector assembly (including cable and strain relief) is contained within the envelope of the board as defined in the PCI specification, the PCI mechanical requirements have been met. The CT Bus connector **MUST** be contained within the PCI envelope.

5.2 Connectors

The connector used on the cable assembly **MUST** be an AMP 1-557089-2 connector or an equivalent from AMP or another manufacturer. On the PCB, either edge fingers or an appropriate mating connector **MAY** be used. If a connector is used on the PCB, it **MUST** be an AMP 1-557100-7 or an equivalent from AMP or another manufacturer.

5.3 Location

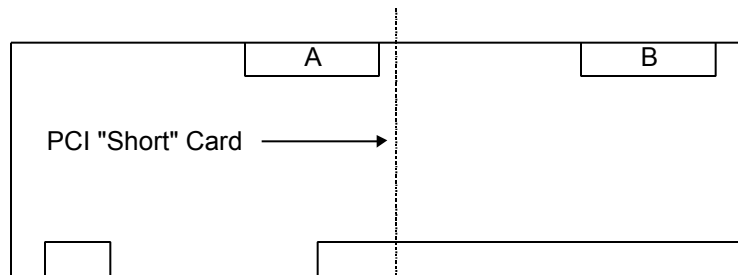


Figure 5-1 Connector Location

There are two possible locations for the CT Bus. The “B” location **MUST** be used for full length PCI cards. The “A” location **MUST** be used on any PCI card that is less than full length.

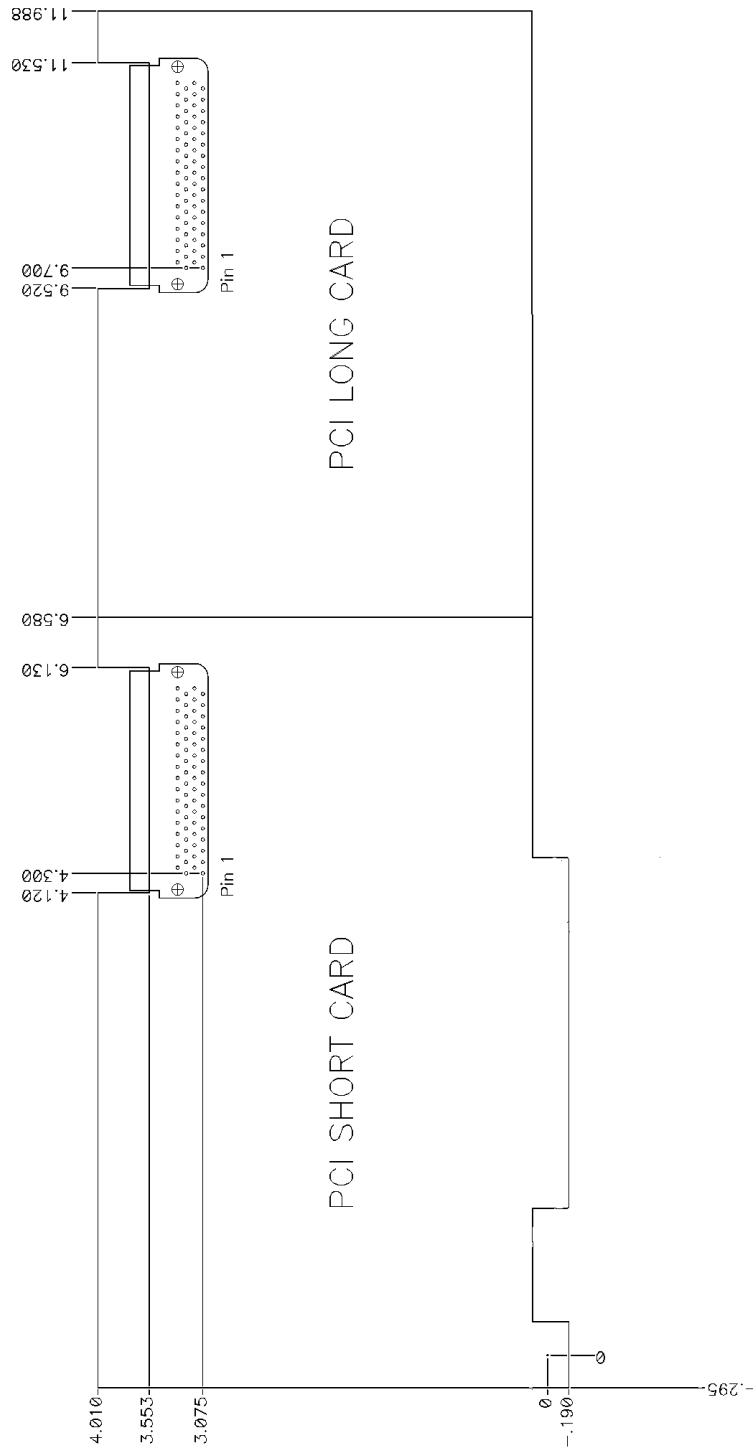


Figure 5-2 PCB Connector Location

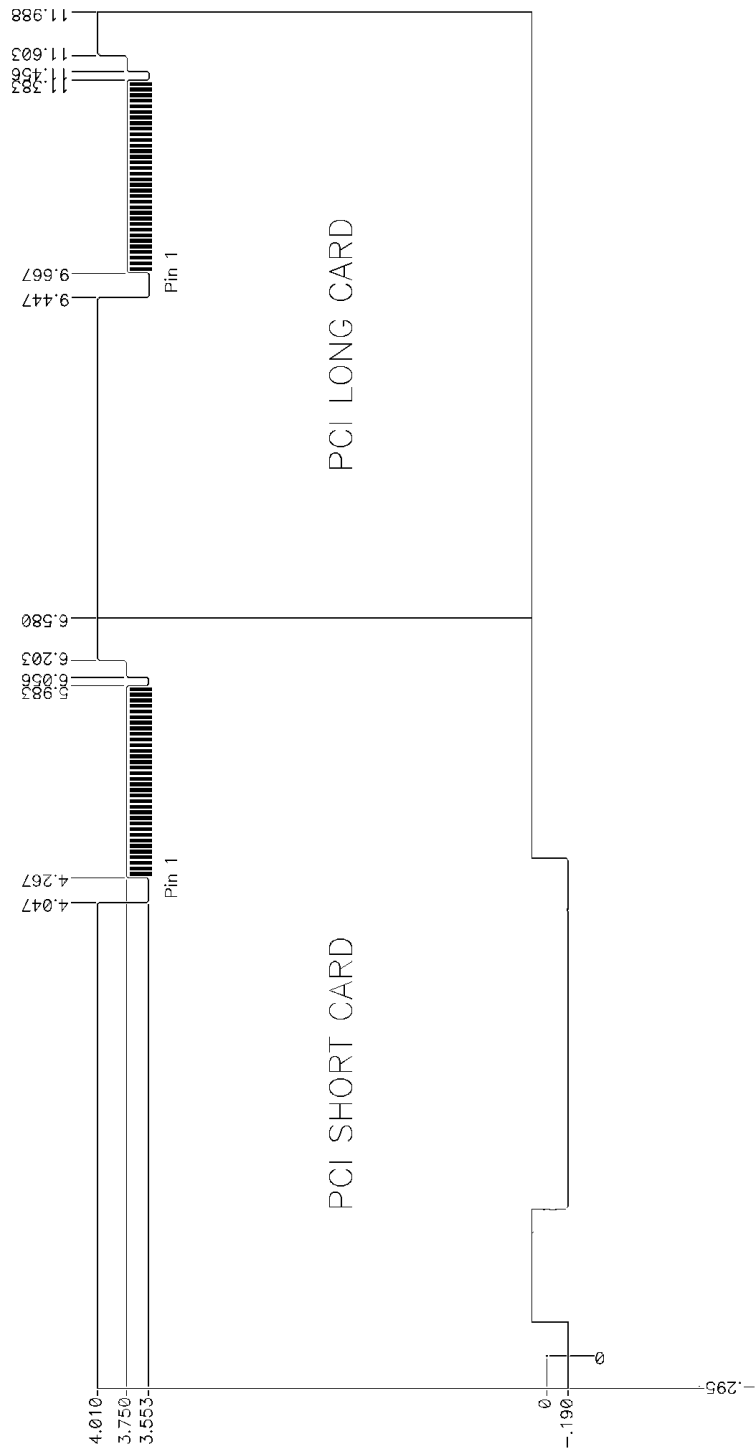


Figure 5-3 PCB Edge-finger Location

5.4 Pin Assignment

Signals are listed as they appear on the connector. Interleaved grounds are present between every four data lines to permit operation at any of the three permitted compatibility bit rates and maximize signal integrity. (See Section 8.) Implementation of “partial” busses MUST begin with CT_D0 and go up sequentially. (See Section 6.)

Table 5-1 Connector Pin Allocation

RESERVED	1	2	CT_+5Vdc
CT_D31	3	4	CT_D30
CT_D29	5	6	CT_D28
GND	7	8	CT_D27
CT_D26	9	10	CT_D25
CT_D24	11	12	GND
CT_D23	13	14	CT_D22
CT_D21	15	16	CT_D20
GND	17	18	CT_D19
CT_D18	19	20	CT_D17
CT_D16	21	22	GND
CT_D15	23	24	CT_D14
CT_D13	25	26	CT_D12
GND	27	28	CT_D11
CT_D10	29	30	CT_D9
CT_D8	31	32	GND
CT_D7	33	34	CT_D6
CT_D5	35	36	CT_D4
GND	37	38	CT_D3
CT_D2	39	40	CT_D1
CT_D0	41	42	GND
/CT_FRAME_A	43	44	GND
CT_C8_A	45	46	GND
CT_NETREF	47	48	GND
/CT_FRAME_B	49	50	GND

Table 5-1 Connector Pin Allocation (continued)

CT_C8_B	51	52	GND
CT_MC	53	54	GND
/FR_COMP	55	56	GND
SCLK	57	58	GND
SCLKx2*	59	60	GND
C2	61	62	GND
/C4	63	64	GND
/C16+	65	66	/C16-
GND	67	68	RESERVED

5.5 PCB Layout and Considerations

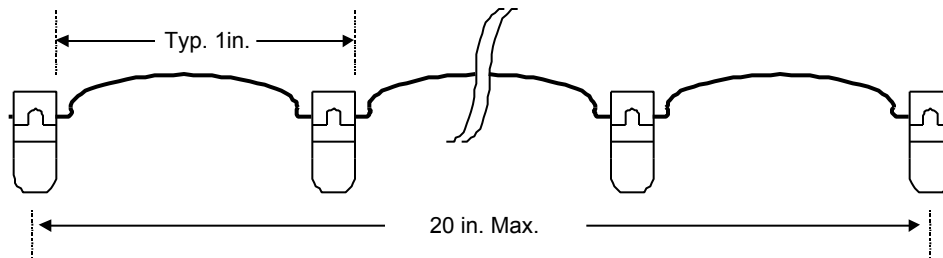
To insure the reliability and consistent performance of the CT Bus, individual CT Bus data lines **MUST NOT** exceed a length of four inches from connector to I/O cell. CT Bus clock lines **MUST NOT** exceed a length of two inches from connector to I/O cell.

5.6 Cable

CT Bus cables **MUST** be constructed from cable having the following characteristics:

Unbalanced Characteristic Impedance:	$90\Omega \pm 5\Omega$
Unbalanced Capacitance:	16 pF/Ft. $\pm 10\%$
Unbalanced Inductance:	0.13 μ H/Ft. $\pm 10\%$

3M 3756 (TPE), 3M 3609 (FEP) or equivalents from 3M, AMP, or other manufacturers satisfy these requirements.


Figure 5-4 Cable Dimensions

5.7 Transition PCBs

Inter-operation with other busses or between long and short H.100 cards might require the use of a transition device. Possible implementations include a folded ribbon cable or a PCB. The design of such a transition device is not provided as part of this document. However, the device forms a part of the CT bus transmission line, and its design will account for the transmission line properties of the CT bus. The device **MUST** be included in the overall bus length calculation. Depending on the loading on the CT Bus and the construction of the transition device, a reduction in the maximum overall cable length can result. It is the responsibility of the provider of the transition device to assess its impact on CT Bus signal integrity. Figure 5-5 shows a possible implementation of a transition device.

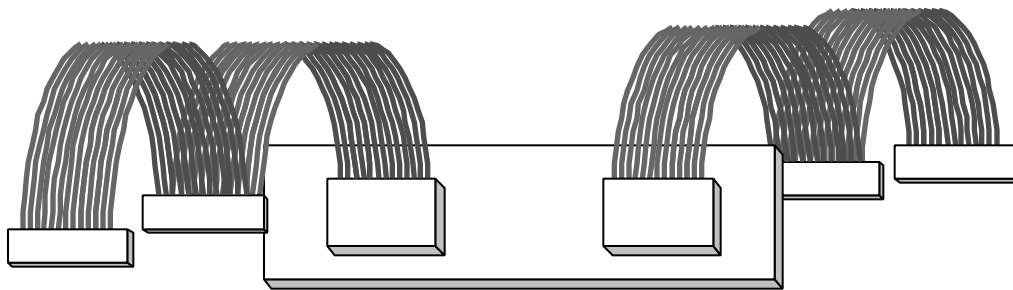


Figure 5-5 Transition PCB

Section 6 : Partial Implementations

6.1 Introduction

CT Bus has been designed with more capacity than any of the previously deployed buses. This is useful for high capacity systems, however there is a cost associated with a full implementation which cannot be justified in many, otherwise useful, computer-telephony systems. For example, as of 1996, many board-based H.320 video codecs for PCs include one type of line interface directly on the video codec board (typically an ISDN BRI interface). But, to support connections to other types of network services, virtually all such video codecs support a (sometimes optional) TDM bus interface. This allows them to be inter-connected with fractional T1, E1, ISDN PRI, Iso-ethernet, and ATM interfaces in adjacent slots of the same computer. On the other hand, the required interconnection is usually limited to 2 Mbps or less full duplex (typically 384kbps or 768kbps) and one TDM stream or less. When connected in this fashion, the video codec board takes its telecom timing from the bus. It never needs to act as clock master for the bus.

The CT Bus is intended to economically support the widest possible range of applications - from high capacity intelligent peripherals for the public network down to individual video telephony devices. To do this, the CT Bus specification includes well-defined subsets that maximize the opportunity for inter-operation while supporting low-end systems involving as few as two boards.

6.2 Requirements for Partial Implementations

Note that, as indicated in the clocks in section 6.1, boards which do not contain an interface to an external network do not require master clock capability and do not need the ability to drive CT_NETREF. Furthermore, if a device like a video codec includes a BRI interface, but that BRI interface is inactive when the CT Bus interface is in use, then this device can be considered a device without network connections with respect to the CT Bus. It therefore does not need master clock capability.

CT Bus interfaces that connect to less than all 32 data lines **MUST** connect with a contiguous block of data lines beginning with CT_D0. All other data bus requirements **MUST** be met, specifically including tristate requirements.



Section 7 : Optional Signals

7.1 Introduction

The following procedures and the related signals are optional. The interface does not need to implement them in order to be fully H.100 compliant. If, however, the interface implements these procedures and signals, the implementation **MUST** adhere to the requirements which follow.

7.2 Message Channel

7.2.1 Introduction

H.100 also provides a secondary communication medium. It is included as an option to provide low latency and high priority inter-board and -chassis messages. This channel uses a single wire serial bus called the message bus. The message bus protocols are fully defined in ANSI/VITA 6-1994 SCSA in Section 3 (See Ref.2). The message bus operates in a collision sense, multiple access with collision detection (CSMA/CD) access mode. The information transported on the bus is in packet format using the ISO #3309 (HDLC) structure

7.2.2 Message Bus Lines

CT_MC - Message channel - This line contains bit-serial, logical true, NRZ data and is driven with an open collector driver. Data is shifted onto this line with a 2.048MHz clock, referred to as MC clock. See Figure 7-1.

MC Clock - MC clock is used for transmission, reception and collision detection. The relationships among CT_C8, /FR_COMP, CT_MC and MC clock are shown in Figure 7-1.

- MC clock is always 2.048MHz.
- Serial data is put onto signal CT_MC on the rising edge of MC clock.
- Serial data is sampled on CT_MC on the falling edge of MC clock.

MC clock falling edge **SHOULD** be offset from 50:50 symmetry to provide CT Bus settling and setup time for the message bus controllers. This clock timing also provides rejection of cross-talk from the CT_D lines to signal CT_MC that might occur.

Note: MC clock **IS NOT** available on the CT Bus, and needs to be generated on every board that intends to use the message bus.

Figure 7-1 shows the recommended relationship between MC clock and CT_C8. The detailed MC clock timing is covered in figure 7-2 and table 7-1.

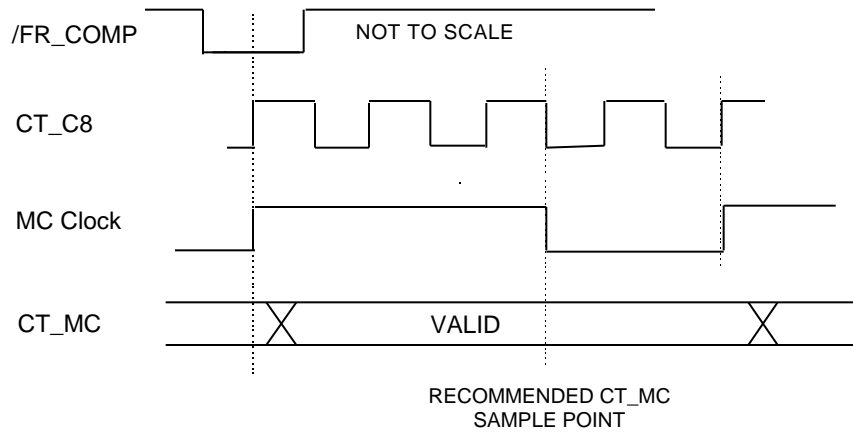


Figure 7-1 Relationship between /FR_COMP, CT_C8, and MC Clock

The MC clock alignment to frame sync shown in figure 7-1 guarantees that all message bus agents are phase-synchronized. This condition is necessary to permit reliable collision detection between message bus modules.

7.2.3 Message Bus - Timing Rules and Observations

The message bus detailed timing relationships is illustrated by the diagram of figure 7-2. Refer to table 7-1 for a description of the detailed timing values for figure 7-2.

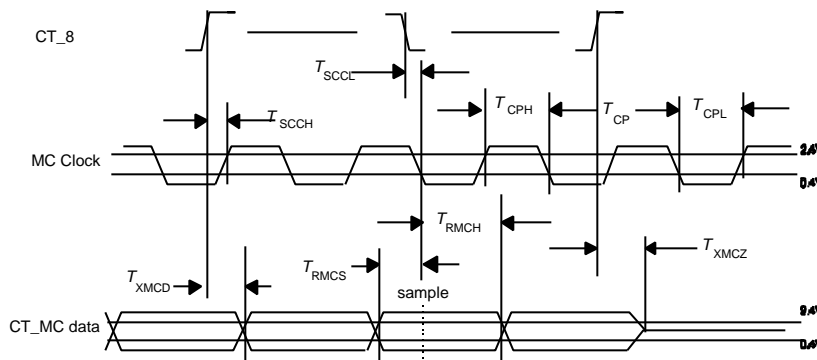


Figure 7-2 Detailed Message Bus Timing

Table 7-1 Message Bus Timing Description

Symbol	Descriptions	Min	Typical	Max	Unit
Tscl	CT_C8 high to MC clock low delay	0		30	
Tscc	CT_C8 high to MC clock high delay	0		30	
Tcph	Clock period high at 2.048MHz	300	305	310	ns
Tcpl	Clock period low at 2.048MHz	168	183	198	ns

Table 7-1 Message Bus Timing Description (continued)

Symbol	Descriptions	Min	Typical	Max	Unit
Tcp	Clock period at 2.048MHz	478	488	498	ns
Txmcd	Output data delay -- from CT_C8 rising edge to valid output or output enabled on the bus. A specification for the transmitter.	0		55	ns
Trmcs	Input data set up time -- from valid data to the falling edge of the MC clock. A specification for the receiver.	25			ns
Trmch	Input data hold time -- from MC clock falling edge until a data change. A specification for the receiver.	30			ns
Txmcz	Output disable delay -- from the CT_C8 rising edge to output disabled. A specification for the transmitter.	0		35	ns

Table Notes

1. Txmcz measured with 220/330 Ω terminator and 20 pF load.

7.2.4 Bus Drivers and Receivers

Message channel equipped boards SHOULD use a TTL-compatible, open-collector type driver with 24 mA or more sinking capability.

The maximum load per board on the bus SHOULD NOT exceed 15 pF capacitance (including the connector).

7.2.5 Bus Terminations

Each CT Bus module MUST provide a 4.7 K Ω pull-up to +5 volts on the CT_MC signal line. Each CT Bus module MUST have all on-board message bus driver outputs tied together and pulled up by one 4.7K Ω resistor. Figures 7-3 and 7-4 illustrate typical methods for driving the SC message bus signal MC.

Each CT Bus module MUST pull up the CT_MC signal as shown in figures 7-3 and 7-4 even if the message bus is not used.

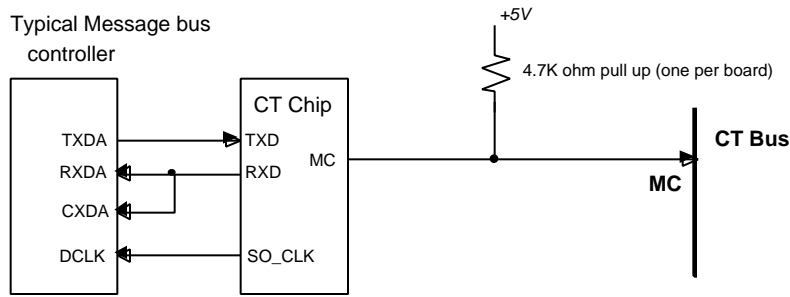


Figure 7-3 Implementation with CT Bus Chip

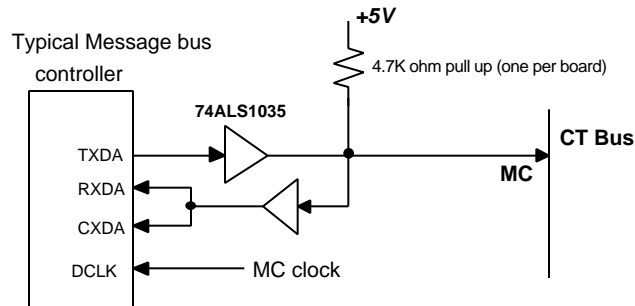


Figure 7-4 Implementation with Discrete Components

7.2.6 DC Characteristics

Table 7-2 contains the DC requirements of the message bus interface devices.

Table 7-2 Message Bus Interface Device Characteristics

Parameter	Symbol	Min	Max	Unit
Operating voltage	V_{CC}	4.75	5.25	Volt
High level input voltage	V_{iH}	2.00	5.25	Volt
Low level input voltage	V_{iL}	-0.25	0.80	Volt
Input leakage current	I_{LH} or I_{LL}		± 10	μA
Output Low current at 0.4V	I_{0L}	24		mA

All input and output requirements are referenced to the CT Bus. Most of the advanced CMOS devices with TTL input threshold level meet the above electrical characteristics.

7.2.7 Loading Limitations

More than 32 drivers **MUST NOT** be connected to one electrical message bus. More than 20 physical boards, each with one termination resistor, **MUST NOT** be connected to one electrical message bus.

7.3 CT_+5Vdc

This signal line is reserved on the bus to permit manufacturers to power transition devices required to interface to their existing busses. The requirements of these active transitions can only be known to their respective manufacturers and are beyond the scope of this document. However, designers employing this signal **MUST** provide short circuit protection so that other parts of the system are not adversely affected by accidental shorting to other signals.



Section 8 : Inter-operation with Other Busses

8.1 Introduction

To aid its widespread adoption, CT Bus has been designed to support easy inter-operation with the following telecom busses: MVIP-90, SCbus, and H-MVIP. Table 8-1 shows the CT Bus signals and their compatibility functions.

Table 8-1 CT Bus Signal Functions

CT Bus	(H-)MVIP Compatibility	SCbus Compatibility	ANSI VITA 6 Compatibility
CT_C8_A			
CT_C8_B			
/CT_FRAME_A			
/CT_FRAME_B			
/FR_COMP	/F0	Fsync*	Fsync*
CT_MC		MC	MC
/C16+	/C16+ (H-MVIP only)		
/C16-	/C16- (H-MVIP only)		
C2	C2		
/C4	/C4		
CT_NETREF	SEC8K	SREF8K	SREF8K
SCLK		SCLK	SCLK
SCLKx2*		SCLKx2*	SCLKx2*
CT_D[0 - 15]	HDS[0 - 15]	SD[0 - 15]	SD[0 - 15]
CT_D[16 -23]	HDS[16 -23] (H-MVIP only)		
CT_D[24 - 31]			

8.2 Common Requirements

CT Bus master-capable interfaces inter-operating with other busses **MUST** support data rates of 2, 4, and 8Mbps. CT Bus master-capable boards **MUST** provide 128 time-slots of bus-to-bus switching at any of the three data rates. CT Bus slave cards inter-operating with other busses

MUST support data rates of 8Mbps and MAY support data rates of 2 and 4Mbps. Table 8-2 shows the interoperability bandwidth between different types of cards.

Table 8-2 Interoperability Bandwidth

Interoperability Agent	Data Rate	Time-slots
CT Bus agent to CT Bus agent (direct)	8 Mbps to 8 Mbps	4096
CT Bus agent to H-MVIP agent (direct)	8 Mbps to 8 Mbps	3072
CT Bus agent to SCbus agent (direct)	8 Mbps to 8 Mbps	2048
CT Bus agent to SCbus agent (direct)	4 Mbps to 4 Mbps	1024
CT Bus agent to SCbus agent (direct)	2 Mbps to 2 Mbps	512
CT Bus agent to MVIP-90 agent (direct)	2 Mbps to 2 Mbps	512
SCbus agent to MVIP-90 agent (direct)	2 Mbps to 2 Mbps	512
SCbus agent to (H-)MVIP agent (Through H.100 switch)	2, 4, 8Mbps to 2, 8Mbps	128 (Minimum Requirement)
SCbus agent to CT Bus agent (Through H.100 switch)	2, 4, 8Mbps to 8Mbps	128 (Minimum Requirement)
(H)MVIP agent to CT Bus agent (Through H.100 switch)	2, 8Mbps to 8Mbps	128 (Minimum Requirement)

Figure 8-1 shows an example mixed system with the possible data paths and clock distribution. Dashed lines represent optional paths.

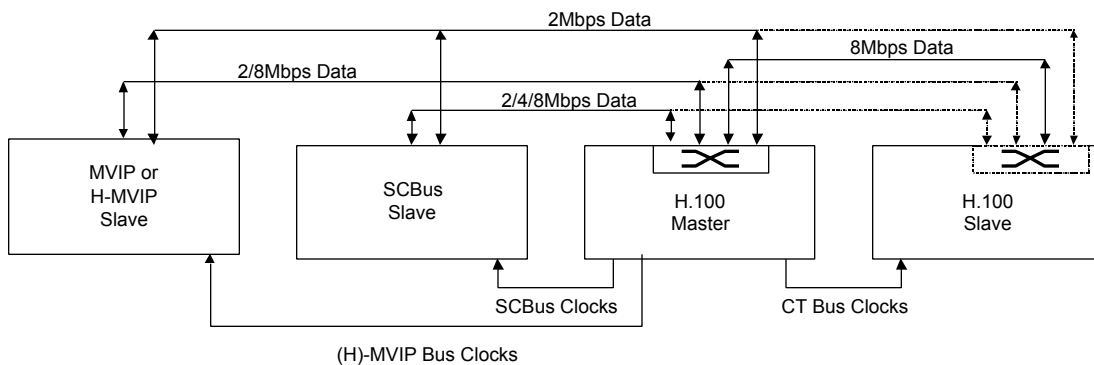


Figure 8-1 Compatibility Data Paths and Clocks

Stream groups [0:3],[4:7],[8:11], and [12:15] MAY be independently operated at any of the three permitted data rates. Depending on the target bus, some data lines will need to operate at different data rates. Figure 8-2 shows the functional timing of the different data rates.

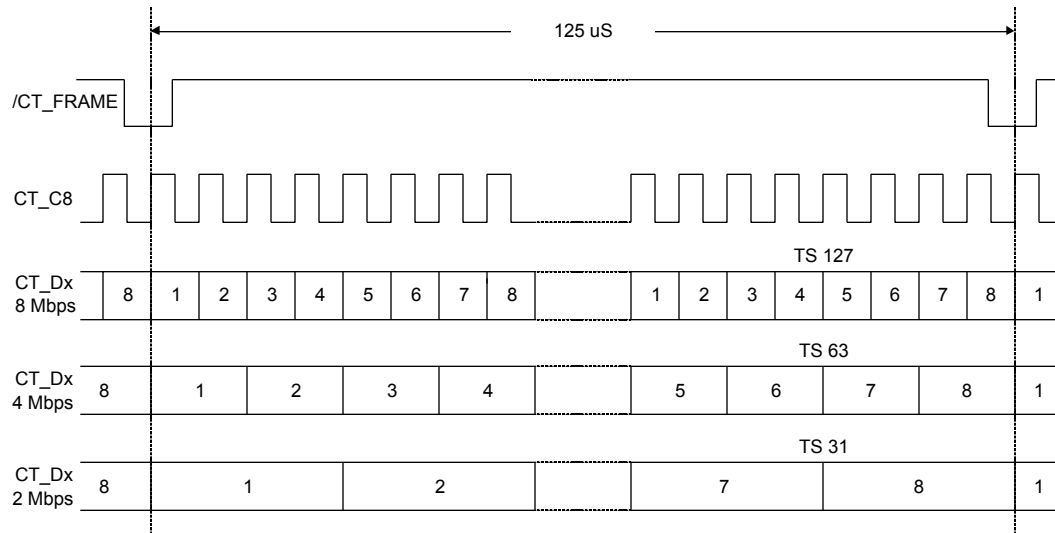


Figure 8-2 Functional Timing for 8, 4, and 2 Mbps Data Streams

Table 8-3 shows the permitted rates for each stream.

Table 8-3 Inter-operability Data Rates

Streams	Interoperability Data Rates
0 - 3	2, 4, and 8 Mbps.
4 - 7	2, 4, and 8 Mbps.
8 - 11	2, 4, and 8 Mbps.
12 - 15	2, 4, and 8 Mbps.
16 - 31	8 Mbps.

A CT Bus interface **MUST** be the clock master and **MUST** provide the compatibility clocks for H-MVIP and SCbus. The multiple data rate requirements for those two busses are defined in the following sections. For cases where active circuitry is required to perform translation between busses, one 5Vdc line is optionally available to power active circuitry on the translation device.

8.3 H-MVIP

The CT Bus **MAY** be connected to an H-MVIP bus by using a passive transition device described in section 5.7. The total cable length, including the transition device, is still limited to 20 inches. One of the defined modes of operation for H-MVIP is MVIP-90. H-MVIP compliance guarantees MVIP-90 compliance. (See Ref. 6).

8.3.1 Clocks

The mapping between the CT Bus and H-MVIP is as follows:

Table 8-4 CT Bus to H-MVIP Bus Mapping 8.3.2 Data Lines

CT Bus	H-MVIP
/FR_COMP	/F0
CT_C8	NC
CT_Dn	HDSn
CT_NETREF	SEC8K
SCLK	NC
SCLKx2*	NC
C2	C2
/C4	/C4
NC	NC
CT_+5Vdc	NC

For H-MVIP the following five modes of operation are defined:

1. 3072 time-slots:
 - All streams operate at 8Mbps
2. 2560 time-slots:
 - Streams HDS[0-3] are operated at 2Mbps as MVIP-90 streams DSo0, DSi0, DSo1, and DSi1. Stream HDS4 is grounded at every H-MVIP interface and streams HD[5-23] are operated at 8 Mbps.
3. 1536 time-slots:
 - HDS[0-15] are operated at 2 Mbps as a standard MVIP-90 bus and streams
 - HDS[16-23] are operated at 8 Mbps.
4. 768 time-slots:
 - All streams operate at 2 Mbps.
5. 512 time-slots
 - Sixteen streams operate per the MVIP-90 specification.

For each of the above modes HDS[0-23] map to CT_D[0-23]. Note that in mode (2) above HDS4 is pulled directly to ground on each H-MVIP bus card. If the user wishes to have CT_D4 available for time-slot transport on the CT Bus side, a jumper MUST be included on the transition device to break the connection between HDS4 and CT_D4. All grounds SHOULD be

terminated in a common ground on the transition device. Unused lines from the CT Bus side MUST be “no connects”.

8.4 SCbus

The 68 pin CT Bus can be cabled to SCbus-equipped boards via the use of a suitable cabling adapter. The adapter connects the appropriate SCbus signals on the CT Bus cable (see section 5.4) to the appropriate pins of a 26 conductor ribbon cable that connects the SCbus cards.

Note that CT Bus drivers are PCI compliant, while SCbus drivers are required to drive 24 mA. Therefore, the design of the CT Bus clock master card will determine if the SCbus specified length of 21 inches can be obtained.

8.4.1 Signal Cross Reference

The mapping between CT Bus and SCbus is as follows:

Table 8-5 CT Bus to SCbus Mapping

CT Bus	SCbus
/FR_COMP	Fsync*
CT_C8	NC
CT_Dn	SD n
CT_NETREF	SREF8K
SCLK	SCLK
SCLKx2*	SCLKx2*
C2	NC
/C4	NC
CT_MC	MC
CT_+5Vdc	NC

8.4.2 Clock Compatibility

The CT Bus clock master module drives all CT Bus clocking signals within their respective specifications so as to provide inter-vendor interchange of TDM data. However, TDM data can only be directly exchanged between modules that support the same CT_D data rates.

Since there is only one set of SCbus clock signals, SCLK and SCLKx2*, all SCbus cards MUST use the same serial data rate. Some older SCbus cards might not support 8.192MHz as an option and will only be capable of directly interchanging SCbus data at 2.048 or 4.096 MHz. SCbus cards that provide only 4.096MHz clocking can only directly exchange TDM data with other 4.096MHz data rate cards. For CT bus systems with different data rate cards installed, the CT_D lines will need to be segregated by data rate (see section 8.2) and direct interchange can only

take place between cards using the same rate. Also notice that the ribbon cable signal terminations might need to be adjusted accordingly.

The timing of SCLKx2* follows figure 8-3 and table 8-6 when SCbus is operating at 8.192 MHz.

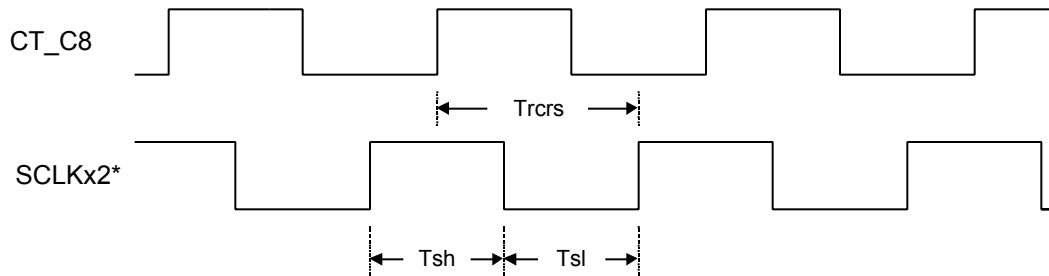


Figure 8-3 SCLKx2* Timing for SCbus Operating at 8.192MHz.

Table 8-6 SCLKx2* Timing for SCbus Operating at 8.192MHz

Symbols	Parameter	Min.	Typ	Max	Unit
Trcrs	Rising Edge of CT_C8 to Rising Edge of SCLKx2*	86.5	91.5	96.5	ns
Tsh	SCLKx2* High Time	51	61	71	ns
Tsl	SCLKx2* Low Time	51	61	71	ns

Table Notes

1. Rising edge of CT_C8 to Rising edge of SCLKx2* includes ± 5 nS of skew as with other compatibility signals.
2. SCLKx2* high and low times indicate nominal $\pm\Phi$.

Appendix A : V/I Curves for 24mA Drivers Used in CT Bus Simulations

Spice simulations of the CT Bus signals CT_C8 and /CT_FRAME were based on a 24 mA VLSI driver cell “ps5b07s”. Process parasitic files are referenced under a library named “CMN6”. The curves below were generated from this information and represent the “fastest”, “typical” and “slowest” curves for that device.

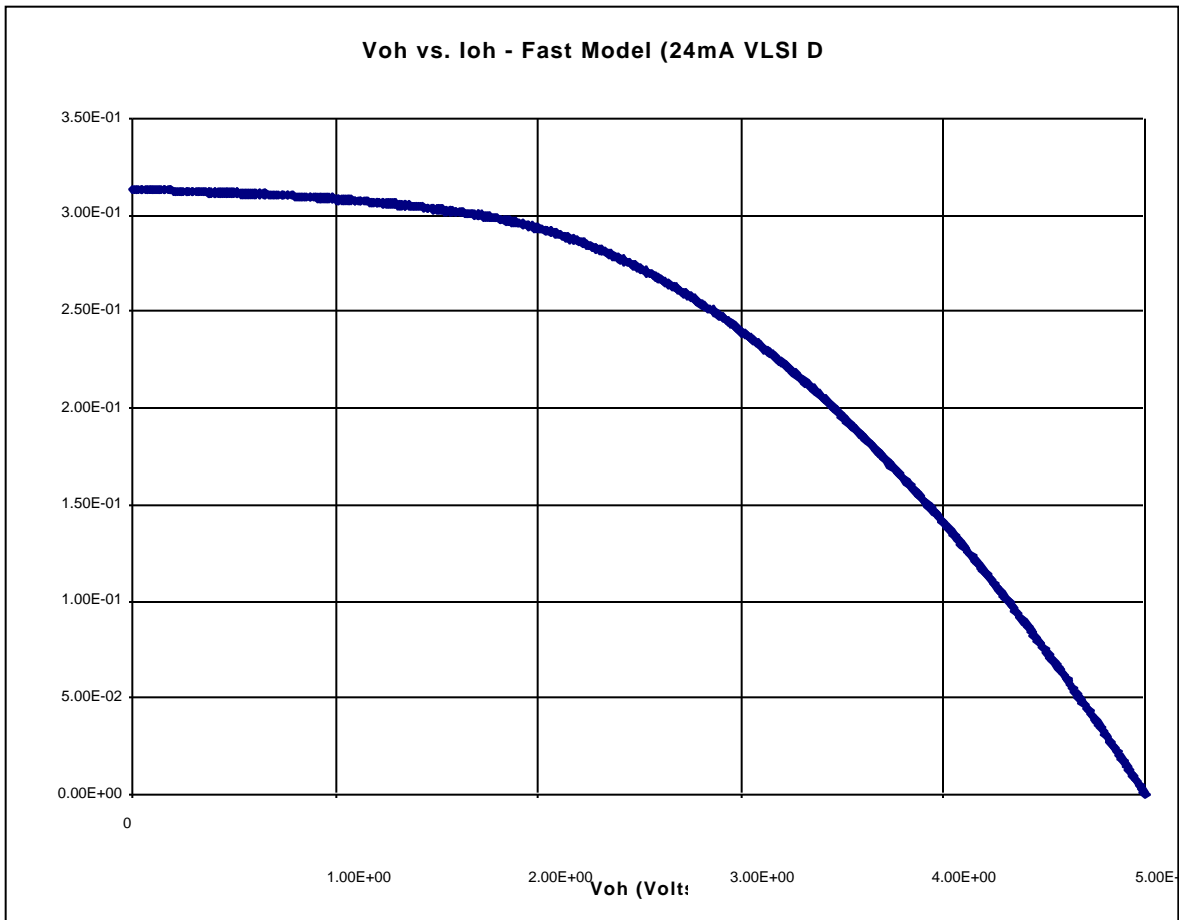


Figure A-1 Voh vs. Ioh - Fastest Model

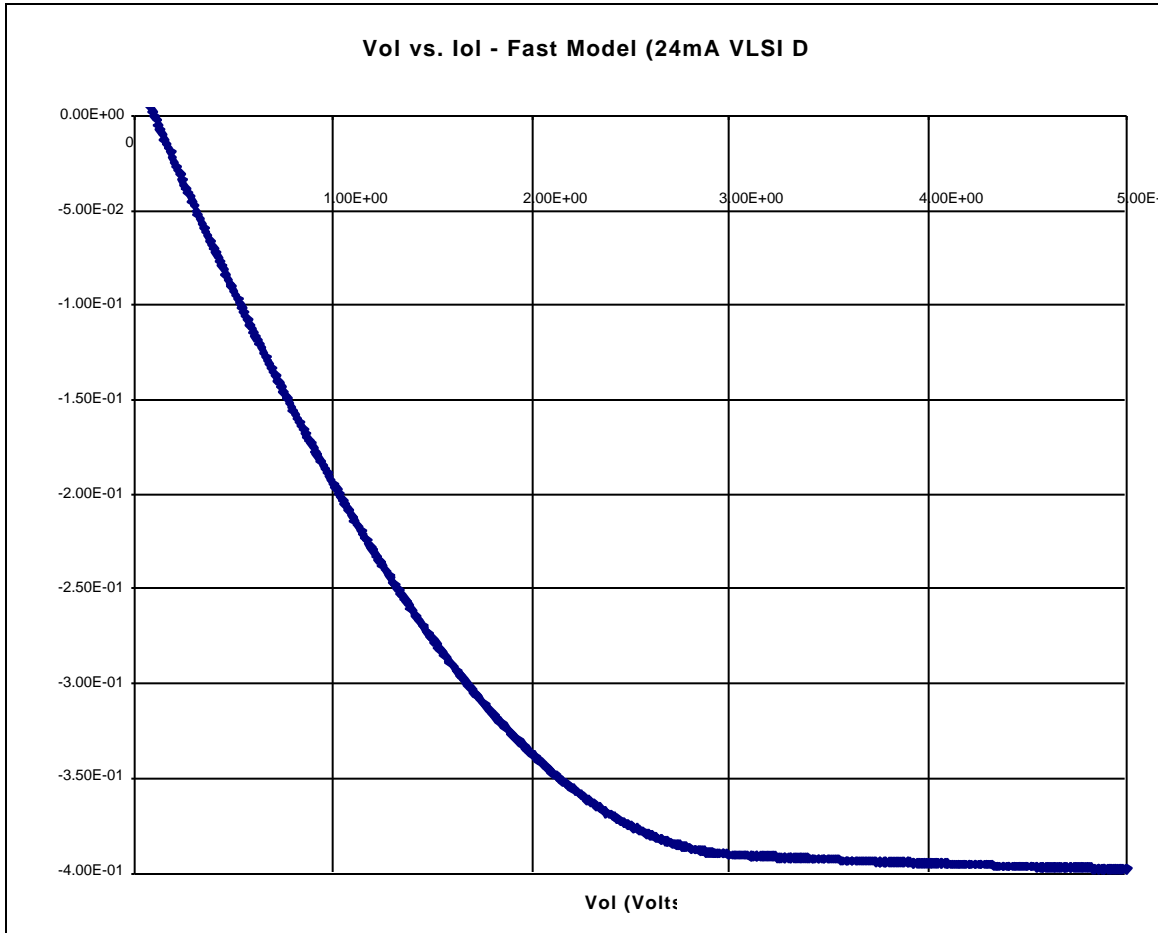


Figure A-2 Vol vs. Iol - Fastest Model

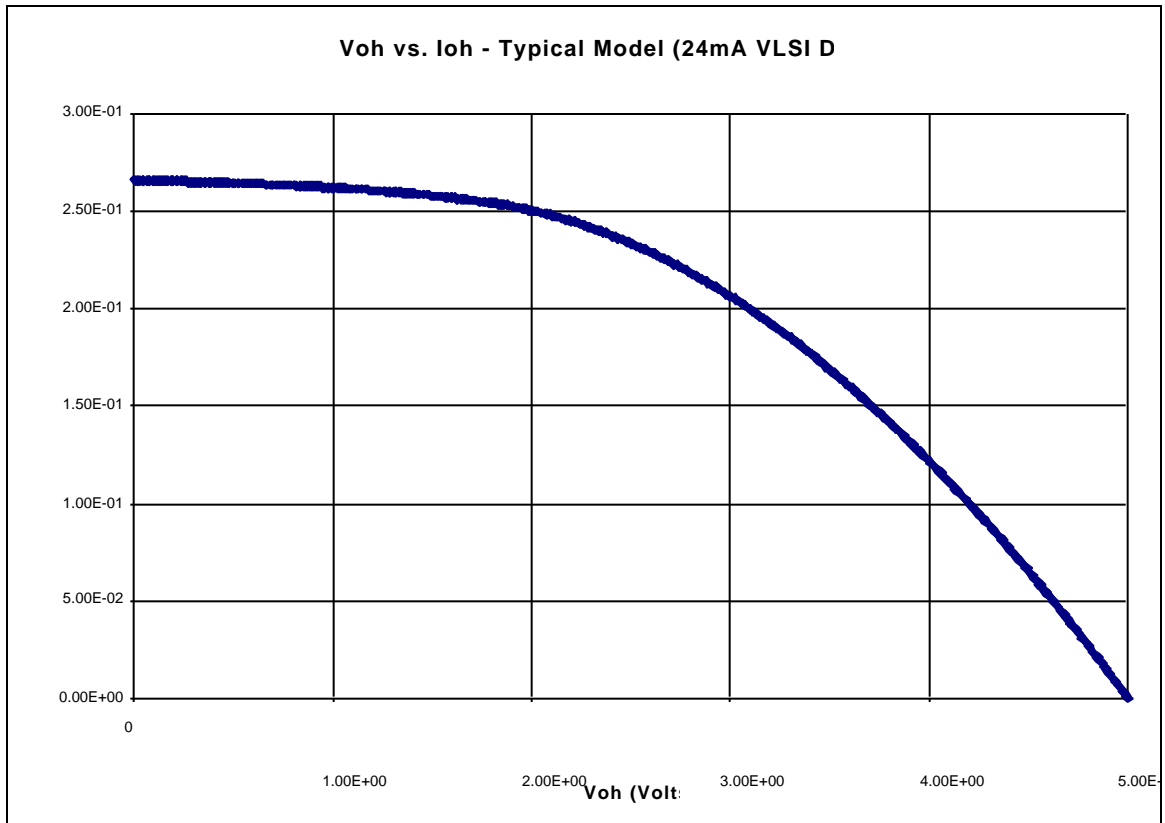


Figure A-3 Voh vs. Ioh - Typical Model

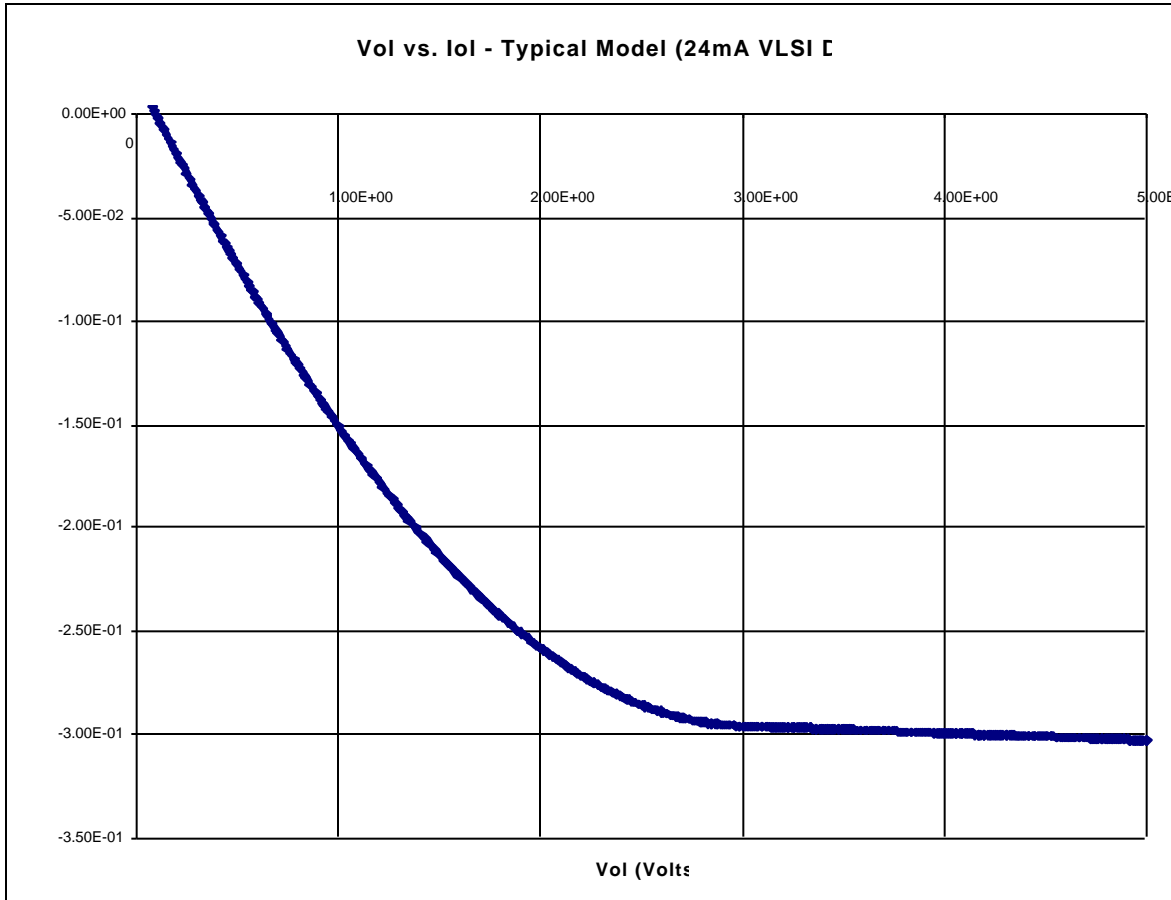


Figure A-4 Vol vs. Iol - Typical Model

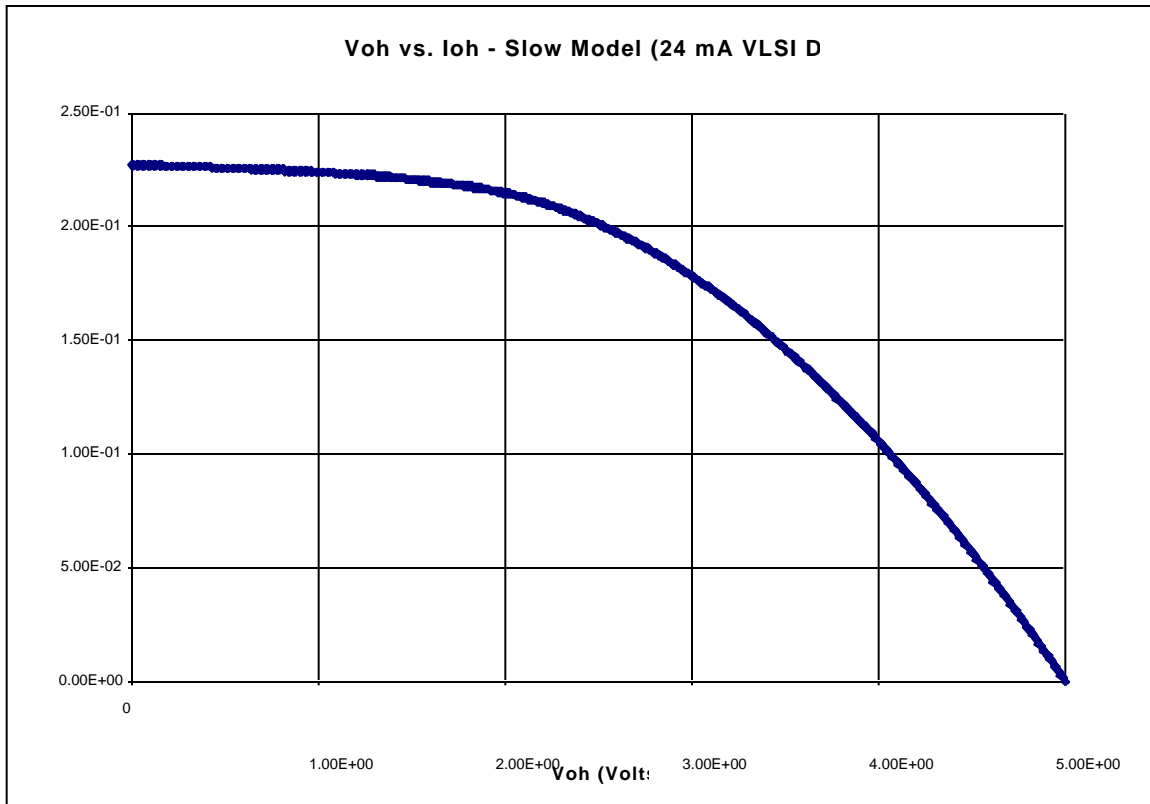


Figure A-5 Voh vs. Ioh - Slowest Model

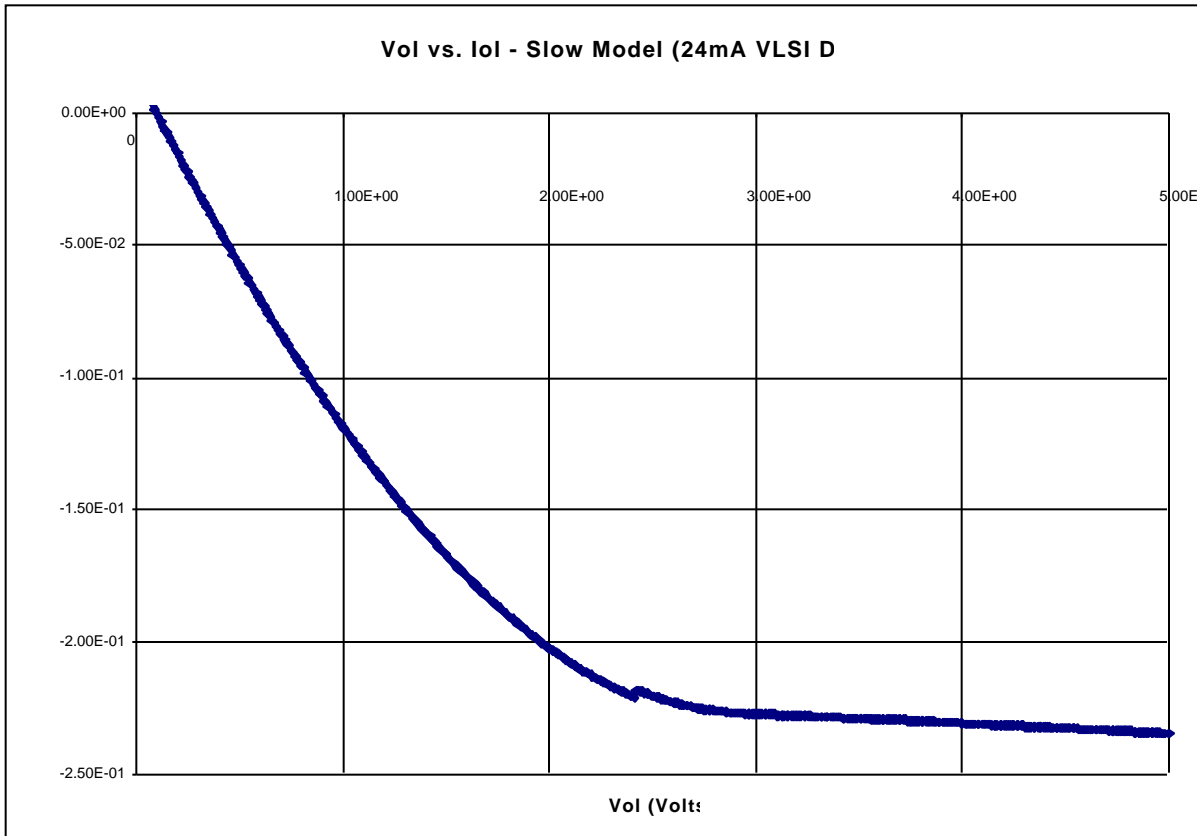


Figure A-6 Vol vs. Iol - Slowest Model